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FinFET Modeling for IC Simulation and Design. FinFET Modeling for IC Simulation and Design. Using the BSIM-CMG Standard. 2015, Pages 157-194. Chapter 7 - Parasitic resistances and capacitances. ... A bird's-eye view of the FinFET simulation structure is shown in Figure 7.12. Because of symmetry, only one-half of the FinFET needs to be simulated.

Parasitic resistances and capacitances - ScienceDirect

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FinFET Modeling and Extraction at 16-nm - SemiWiki

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Explains FinFET modeling for IC simulation and the industry standard for FinFET modeling - BSIM-CMG. This book gives a foundation on the physics and operation of FinFET, explaining the need to go from planar to 3D architecture. It then covers detailed aspects of the BSIMCMG model such as surface potential, charge and current calculations.

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